AMENDMENTS TO THE DRAWINGS

The attached drawing sheets includes a newly presented Fig.4 based on the description provided in the specification on page 14 line 24 through page 15 line 8. No new matter has been entered. A substitute sheet for Figure 3 has also been included re-labeling Figure 3 as "RELATED ART".

Attachments: New Drawing Sheet – Figure 4, substitute sheet Figure 3.

REMARKS

Claims 1-8 are pending in the present application. Reconsideration in view of the above amendment and the following remarks is respectfully requested.

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicants further acknowledge and appreciate receiving an initialed copy of the form PTO-1449 submitted in connection with the Information Disclosure Statement filed on August 4, 2003.

The drawings were objected to as failing to show the FET embodiment of, for example, claim 8. Applicants have submitted a new Fig. 4 based on the description provided in the specification on page 14, line 24 to page 15 line 8, where it is specifically noted that the bipolar transistors Q11-Q31 of Figure 1 can be replaced with Field Effect Transistors Q11-Q31 as shown in the new Figure 4. It is respectfully submitted that in view of the enabling description, no new matter has been entered. Applicants respectfully request that the new Figure 4 be entered and the objection be removed.

Applicants further respectfully submit that, for example according to 37 C.F.R. § 1.81, drawings are required in patent application *where necessary for the understanding of the subject matter*. According to 37 C.F.R. § 1.83, the drawings must show every feature of the invention specified in the claims, yet conventional features disclosed in the description and claims, *where their detailed illustration is not essential for a proper understanding of the invention*, should be illustrated in the drawing in the form of a graphical drawing symbol. Field Effect Transistors

(FETs) are clearly described in the specification, for example on page 14, line 24 to page 15 line 8, as being a substitute for bi-polar transistors, for example as shown in Fig. 1 of applicants' specification. Since FETs are well known and thus would not require an illustration to be understood by one of ordinary skill in the art when reading the claim in light of the specification, applicants submit that a separate drawing showing the associated embodiment would not be necessary under 37 C.F.R. § 1.81 or § 1.83. However, to expedite prosecution and to better address the objection, the new Figure 4 has been provided herewith.

Applicants note that further with regard to the objection to the disclosure based on alleged informalities, Figure 3 is alleged to depict prior art. Applicants note that Figure 3 is considered as depicting related art and has accordingly been relabeled as "—RELATED ART—" in the attached replacement sheet. Entry is requested.

Further with regard to the claim objections, applicants submit that the control signal reducing circuit is not the control signal regulating circuit recited, for example in claim 2, as being comprised in the control signal reducing circuit. Therefore applicants have not amended claim 1 as suggested. Claim 6, is objected to for informalities related to the misspelling of "Zener." Claim 6 is amended herein to correct the misspelling.

Claims 1-8 were rejected under 35 USC 112, second paragraph, as being allegedly indefinite. Without admitting the propriety of the rejection the claims have been amended to address issues of clarity for which an objection would have been proper.

It is respectfully submitted that a *prima facie* case of indefiniteness has not been established in that no evidence has been provided to show that one of ordinary skill in the art when reading the claims in light of the specification would have been confused as to the meaning of the last clause of claim 1. Merely asserting that the claim is poorly worded is insufficient to

establish or sustain an indefiniteness rejection under 35 U.S.C. 112, second paragraph. Applicants submit that claim 1 and in particular the clause, as amended, reciting for example, a control signal reducing circuit configured to reduce the control signal within a range that the driving transistor is kept to the on state when a voltage of the output terminal applied to the driving transistor through the outputting transistor exceeds a predetermined threshold voltage, would have been clear to one of ordinary skill in the art based on a reading of various portions of the specification, for example beginning at page 13, line 7. In particular, the outputting transistor is connected to the output terminal of the operational amplifier and the driving transistor is connected to the outputting transistor.

In this configuration, when the outputting transistor is kept off, a voltage of the output terminal is not applied through the outputting transistor to the driving transistor. When, however, the driving transistor turns on based on a control signal to drive the outputting transistor, the voltage of the output terminal is applied to the outputting transistor, and subsequently applied to the driving transistor from the outputting transistor.. Applicants are convinced that the above description would be clearly understandable to one of skill in the art.

Claim 1 is rejected under 35 USC 102(e) as being allegedly anticipated by Caine, U.S. Patent No. 6,566,957. The applicants respectfully request that this rejection be withdrawn for the following reasons.

In making the rejection, various elements of Figure 13 of Caine are alleged to amount to the claimed features. In particular, n-channel MOSFET 1354 is alleged to amount to the claimed output transistor of the present invention, NPN transistor 1348 is alleged to amount to the claimed driving transistor of the present invention, and NPN and PNP transistors 1344 and 1346 are alleged to amount to the control signal regulating circuit of the present invention.

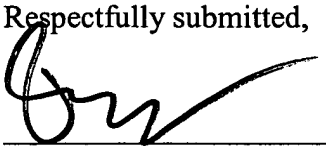
However, as clearly shown in Fig. 13 of Caine, the output signal Vout is not applied through the MOSFET 1354 to the NPN transistor 1348. Therefore, Caine fails to disclose or even teach or suggest that a voltage applied to the NPN transistor 1348 depends on whether the output voltage Vout exceeds a predetermined threshold voltage as in the claimed invention.

In claim 1 of the present invention, as amended, the operational amplifier is configured such that the voltage of the output terminal is applied to the driving transistor through the outputting transistor, and consequently the voltage applied to the driving transistor depends on whether the voltage of the output terminal exceeds the predetermined voltage. Accordingly, Caine is structurally different in relation to claim 1 of the present invention as amended, and, as noted above, Caine fails to disclose features thereof. It is respectfully requested that the rejection of claim 1 be reconsidered and withdrawn. Claims 2-8, by virtue of depending from claim 1, are allowable for at least the reasons set forth herein above.

In view of the foregoing, the applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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